



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/718,932	11/22/2000	Mark Pavier	IR-17732-2498	2141

2352 7590 11/08/2002

OSTROLENK FABER GERB & SOFFEN
1180 AVENUE OF THE AMERICAS
NEW YORK, NY 100368403

EXAMINER

ROMAN, ANGEL

ART UNIT PAPER NUMBER

2812

DATE MAILED: 11/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/718,932

Examiner

Angel Roman

Applicant(s)

PAVIER MARK

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will preserve the right to file.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 13 September 2002
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2 and 5-12 is/are pending in the application
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 5-12 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 22 November 2000 is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f):
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) to a provisional application:
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No.(s) _____
- 4) ☐ Interview Summary (PTO-413) Patent No. _____
- 5) ☐ Notice of Informal Patent Application (PTO-102)
- 6) ☐ Other _____

DETAILED ACTION

Drawings

1. The drawings are objected to because there is an unidentified object adjacent the top die in figure 9 and the drawings of figures 9 and 10 are not clearly legible. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 5, 8, 9 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phy U.S. Patent 4,688,075 in view of Nakabayashi U.S. Patent 6,215,194 B1.

Phy discloses a process of connecting a semiconductor die to a substrate having a top surface, said process comprising the steps of; providing a thin, flexible, heat curable polyimide film 127 which is of a first area; placing said film on a thin semiconductor wafer of a second area, said semiconductor wafer being provided with a

plurality of spaced apart semiconductor die, each of said semiconductor die having a respective third area which is substantially less than said first area (see figure 4); preheating said semiconductor wafer and said film to partially cure said film, thereby forming adhesion between said thin flexible film and said semiconductor wafer (see column 4, lines 50-55); thereafter simultaneously singulating both said thin flexible film and said plurality of identical semiconductor die to form individual elements (see column 4, lines 45-50); thereafter applying at least one of said singulated semiconductor to the top surface of said substrate surface with the film on said die pressed against said top surface and adhered thereto; and thereafter heating said one semiconductor die to fully cure said thin flexible film to firmly adhere said die to said substrate (see column 3, lines 39-45). Said first area is substantially identical to, or different from, said second area (see figure 4). The film on said die has the same or different area as that of said die after assembly onto said substrate. Exemplary materials for the substrate include conductors, metals and alloys (see column 3, lines 21-25). Phy also discloses heating an entire assembly of figure 2B (see column 3, lines 39-45).

Phy is applied as above but lacks anticipation on explaining the die attaching process to substrate 128; disclosing a polyimide insulative material as the adhesive material being used; disclosing the substrate 128 as being comprised of lead; and removing said dice and film to said substrate by a pick and place apparatus.

With respect to explaining the die attaching process to substrate 128 Nakabayashi discloses a die attaching process comprising preheating a substrate before attaching a die using a polyimide adhesive and further heating the attachment to

Art Unit: 2812

fully cure the adhesive (see column 6, lines 1-36). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use the die attaching process disclosed in Nakabayashi in the primary reference of Phy, since adhesion between the adhesive polyimide layer and the substrate may be improve.

Regarding disclosing a polyimide insulative material as the adhesive material being used, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to use polyimide insulative adhesive in the primary reference of Phy if device insulation is desire (see Applicants Specifications page 1, lines 12-15).

With respect to disclosing the substrate 128 as being comprised of lead Phy suggest using a substrate comprising conductive material (see column 6, lines 28-30). In view of this disclosure it would have been obvious to one having ordinary skills in the art at the time the invention was made to used a substrate comprising lead since lead is a conductive material, furthermore mounting semiconductor dies on lead substrate is widely used in conventional semiconductor packaging procedures.

As to removing said dice and film to said substrate by a pick and place apparatus, Nakabayashi discloses removing a dice and film to a substrate using a pick and place apparatus (see figure 1D). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to remove the dice and film to said substrate by a pick and place apparatus in the

primary reference of Phy as using the pick and place method disclosed in Nakabayashi since process cost may be reduce by improving productivity.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Phy U.S. Patent 4,688,075 in view of Nakabayashi U.S. Patent 6,215,194 B1 as applied to claims 1, 2, 5, 8, 9 and 12 above, and further in view of Burns U.S. Patent 5,221,642.

Phy as modified by Nakabayashi is applied as above but lacks anticipation on adhering a second semiconductor die with a second adhesive film thereon to said substrate at a position laterally remove from a first die, Burns discloses adhering a second semiconductor die with a second adhesive film thereon to a substrate at a position laterally remove from a first die (see figure 4b). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to adhere a second semiconductor die with a second adhesive film thereon to a substrate at a position laterally remove from a first die as disclose in Burns in the primary reference of Phy as modified by Nakabayashi because it is a conventional form of arranging dies on substrates in the semiconductor manufacturing industries.

5. Claims 7, 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phy U.S. Patent 4,688,075 in view of Nakabayashi U.S. Patent 6,215,194 B1 as applied to claims 1, 2, 5, 8, 9 and 12 above, and further in view of Takiar et al. U.S. Patent 5,442,435.

Phy as modified by Nakabayashi is applied as above but lacks anticipation on adhering a second die with a second adhesive film thereon to the top of said die secured to said substrate and a process wherein said adhesive film has a smaller area than said top surface of said die and wherein said second die and said second adhesive film both have the same area as said adhesive film.

With respect to adhering a second die with a second adhesive film thereon to a top of a die secured to a substrate, Takiar et al. discloses adhering a second die with a second adhesive film thereon to a top of a die secured to a substrate (see figure 3). In view of this disclosure it would have been obvious to a person having ordinary skills in the art at the time the invention was made to adhere a second die with a second adhesive film thereon to a top of a die secured to a substrate as disclose in Takiar et al. in the primary reference of Phy as modified by Nakabayashi since manufacturing costs may be reduced.

Regarding a process wherein an adhesive film has a smaller area than a top surface of a die and wherein a second die and a second adhesive film both have the same area as said adhesive film. This limitation, is only considered to be an obvious modification of the shape of the area disclosed by Takiar et al. as the courts have held that a change in shape or configuration, without any criticality, is within the level of skill in the art as the particular shape claimed by applicant is nothing more than one of numerous shapes that a person having ordinary skill in the art will find obvious to provide using routine experimentation based on its suitability for the intended use of the invention. See In re Dailey, 149 USPQ 47 (CCPA 1976).

Response to Arguments

6. Applicant's arguments with respect to claims 1, 2 and 5-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Tsukagoshi et al. and Kata et al. disclose methods for attaching semiconductor dies to substrates using heating processes with polyimide adhesives. Unno et al. and Koniya et al. disclose methods for dicing semiconductor wafers by attaching polyimide adhesives to the wafers before dicing and afterwards attaching dies obtained from the dicing process using the polyimide adhesives.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Application/Control Number: 09/718,932

Page 8

Art Unit: 2812

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
November 4, 2002

A handwritten signature in black ink, appearing to be "J. Kelly", written in a cursive style.